

**FIG.1**

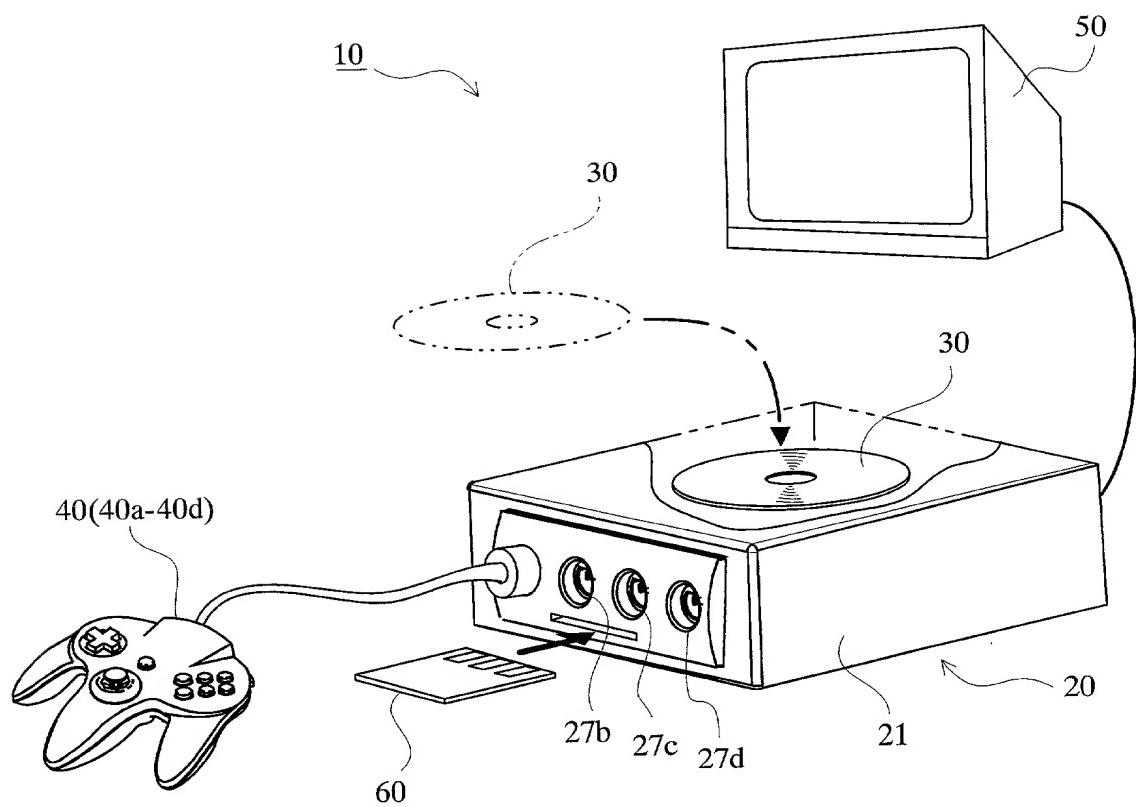
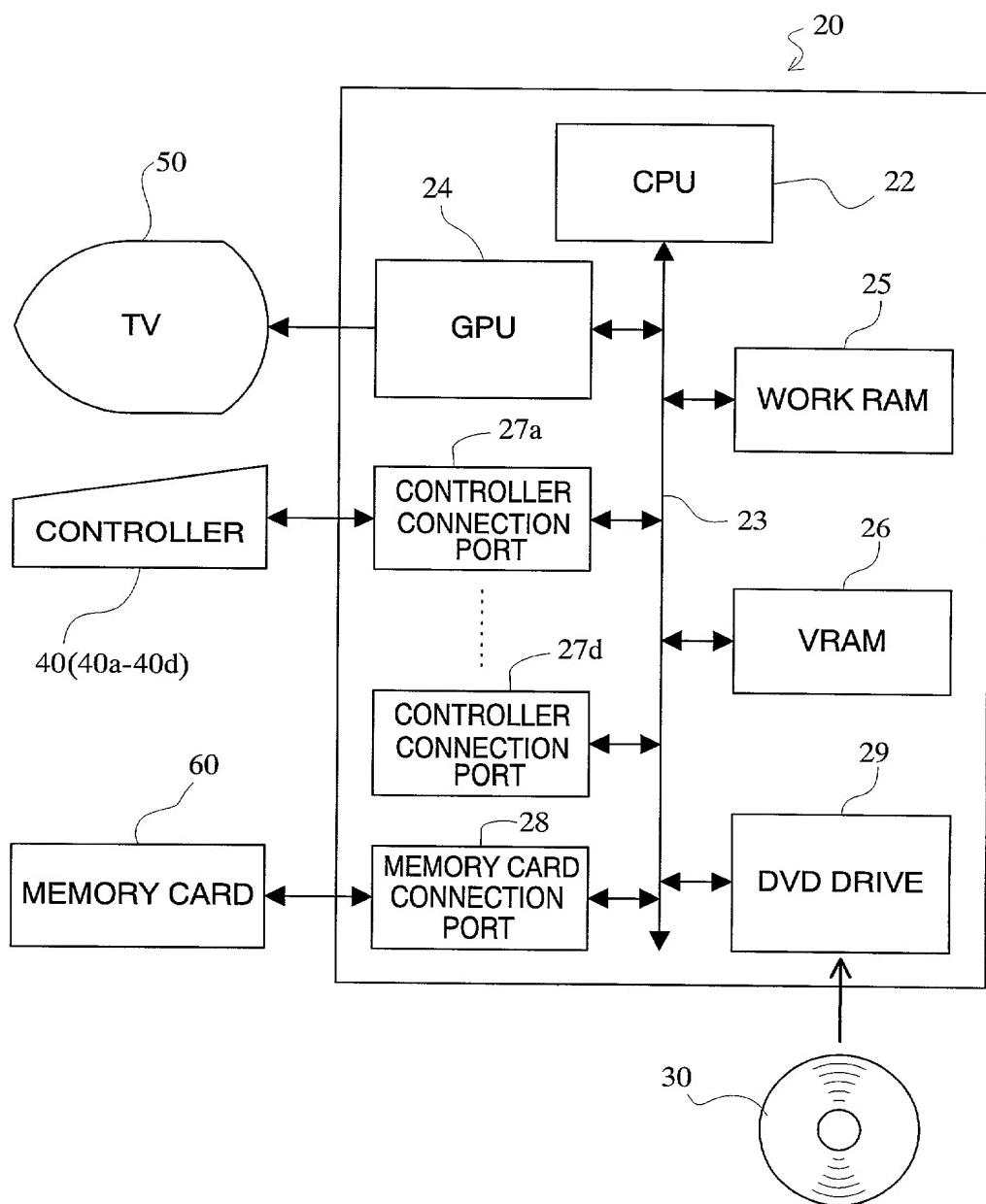


FIG.2



**FIG.3**

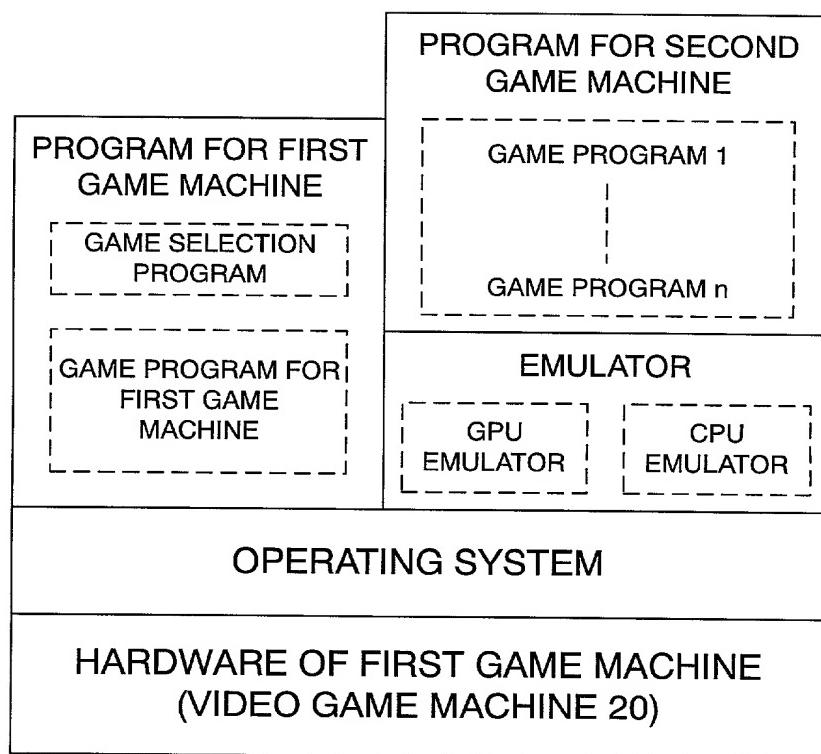
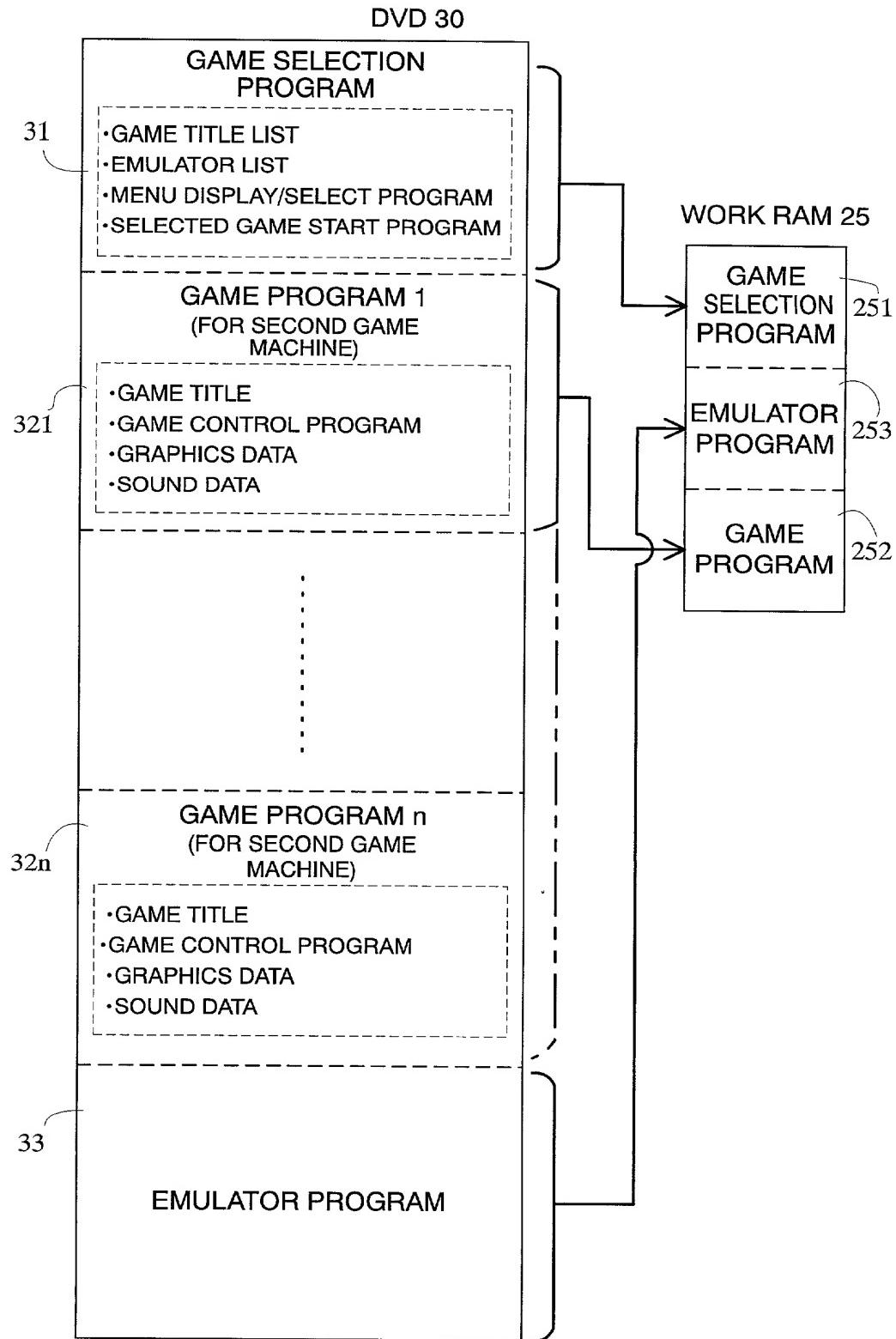
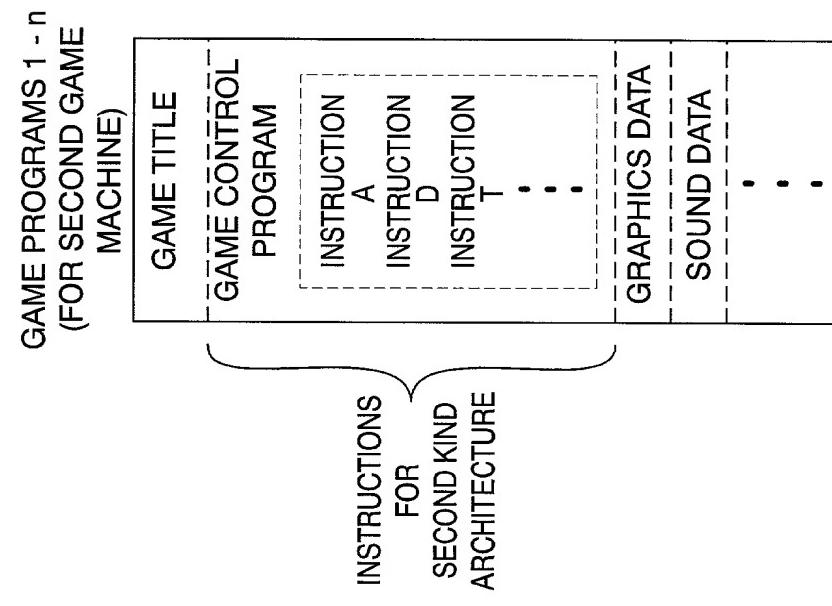


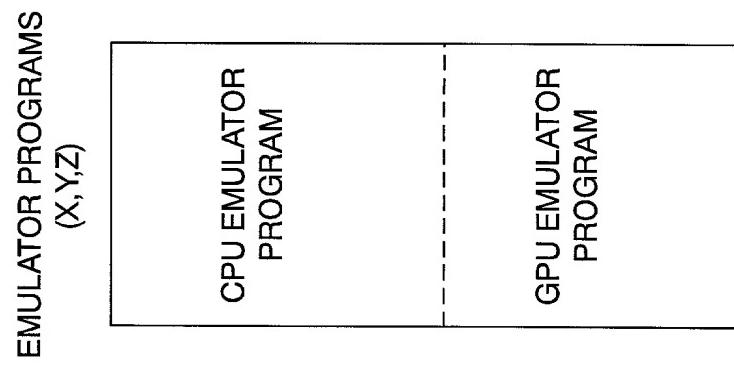
FIG.4



**FIG.5A**



**FIG.5B**



**FIG.5C**

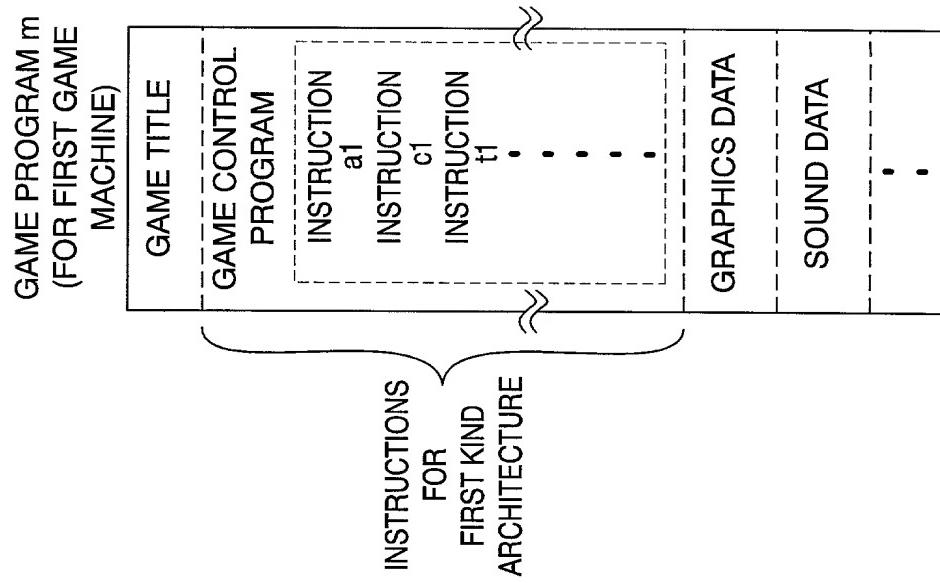
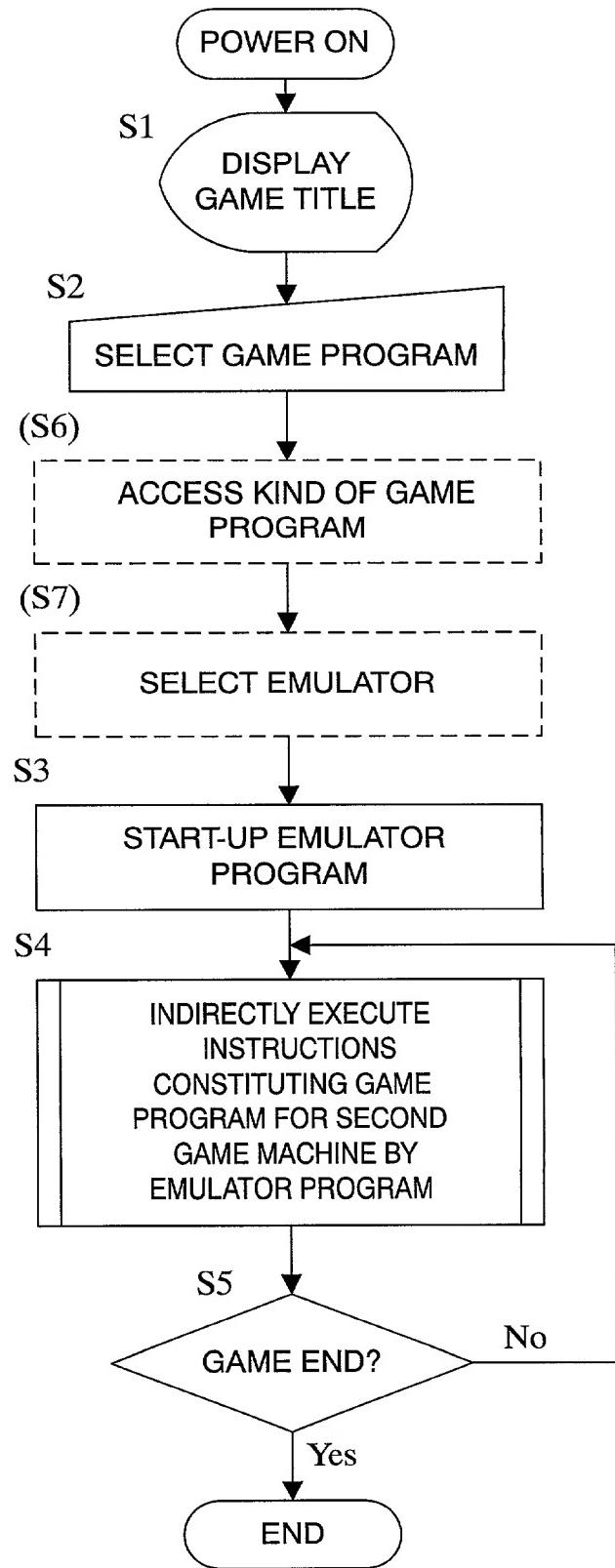


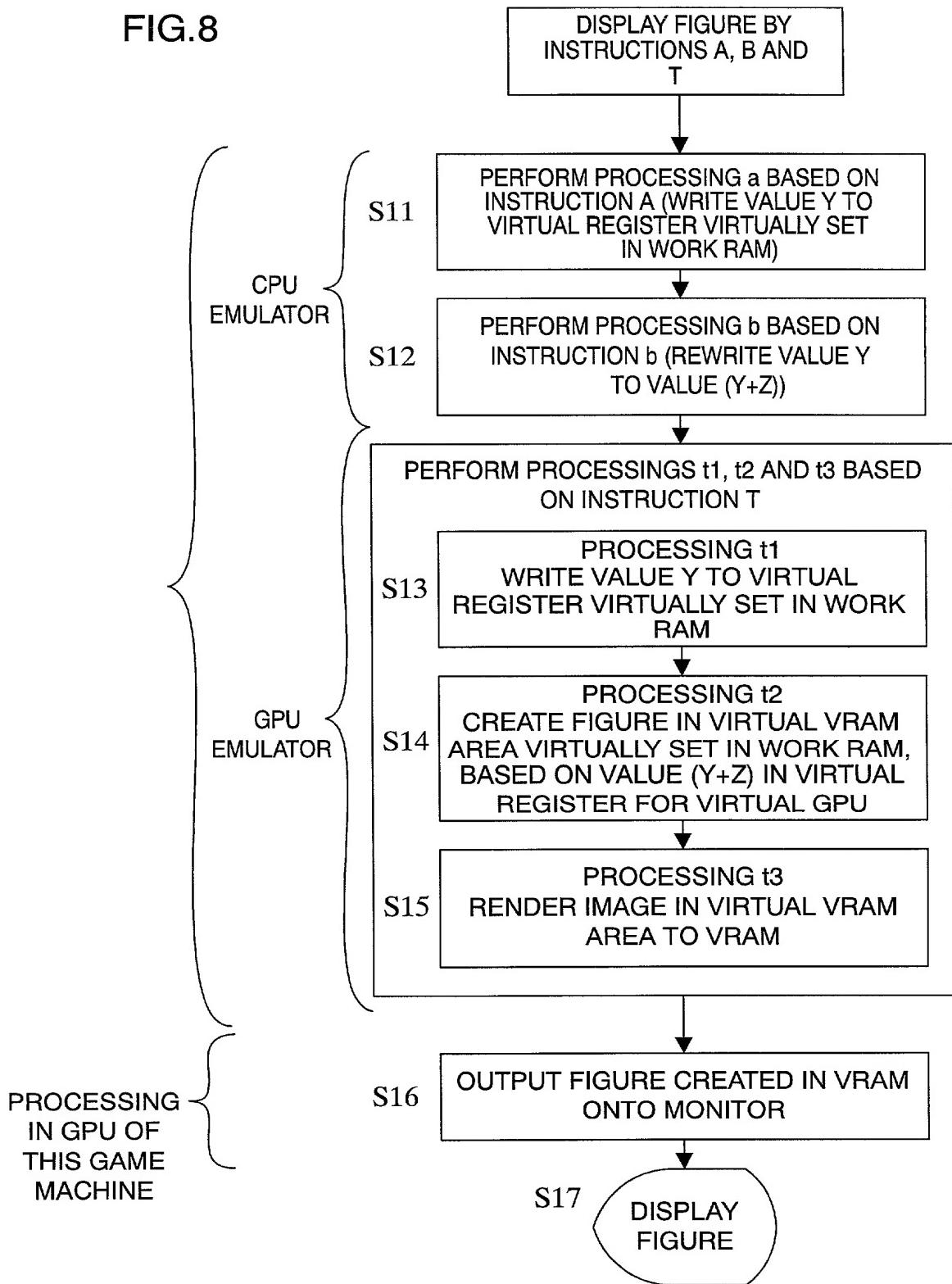
FIG.6

EMULATOR PROGRAM		
INSTRUCTIONS CONSTITUTING GAME PROGRAM FOR SECOND GAME MACHINE (INSTRUCTIONS OF SECOND KIND ARCHITECTURE)	CPU EMULATOR (INSTRUCTIONS OF FIRST KIND ARCHITECTURE)	GPU EMULATOR (INSTRUCTION OF FIRST KIND ARCHITECTURE)
INSTRUCTION A	PROCESSING <sub>a</sub> (INSTRUCTIONS a1,a2,a3)	—
INSTRUCTION B	PROCESSING <sub>b</sub> (INSTRUCTION b1)	—
INSTRUCTION J	PROCESSING <sub>j</sub> (INSTRUCTIONS j1,j2)	—
INSTRUCTION K + INSTRUCTION L	PROCESSING <sub>kl</sub> (INSTRUCTION kl)	—
INSTRUCTION T (EXCLUSIVE INSTRUCTION FOR GPU)	—	PROCESSING t1 {PROCESSING t2 {PROCESSING t3 (INSTRUCTIONS t11,t12,...)}
INSTRUCTION U (EXCLUSIVE INSTRUCTION FOR GPU)	—	PROCESSING u (INSTRUCTIONS u1,u2,u3)

FIG.7



**FIG.8**



**FIG.9**

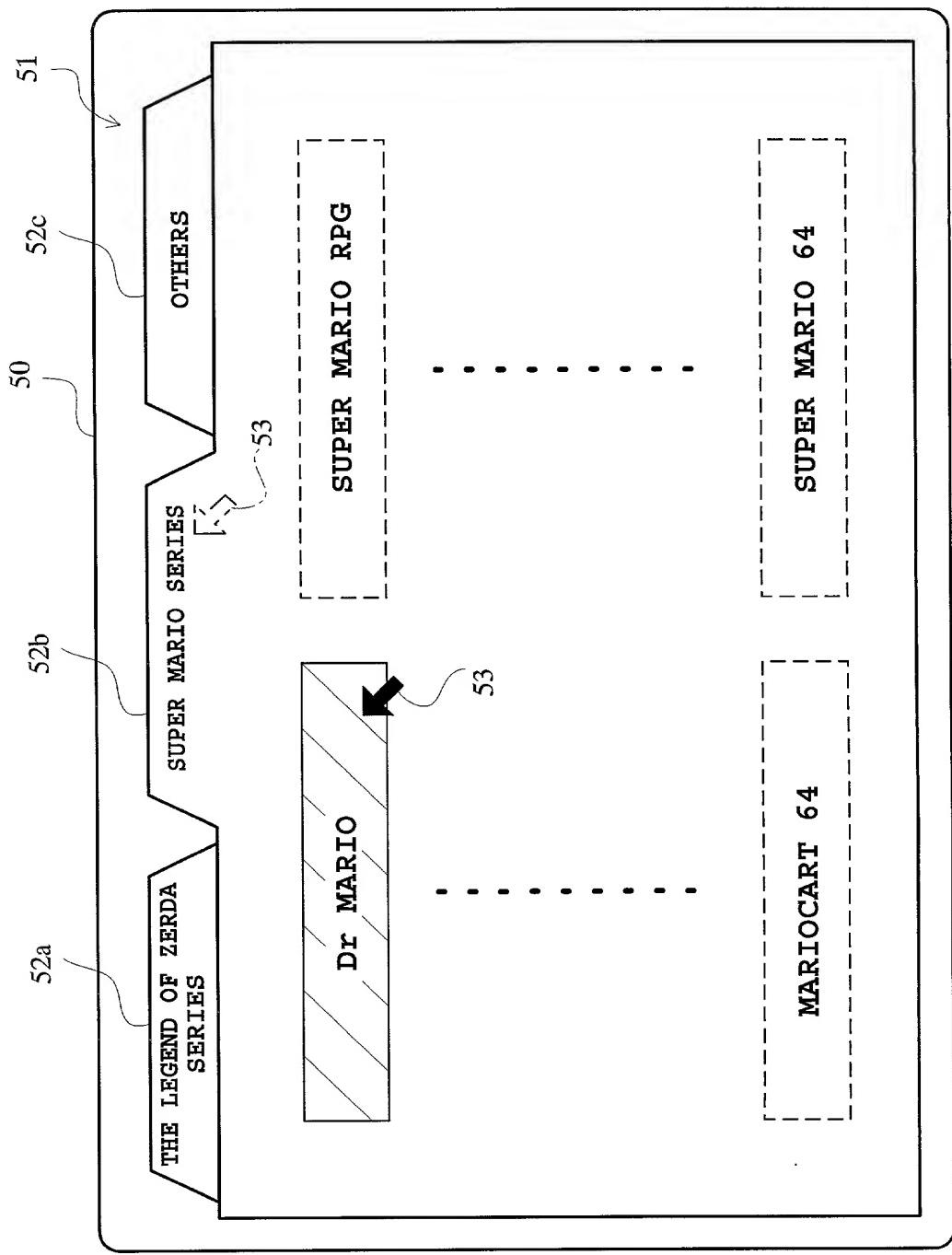
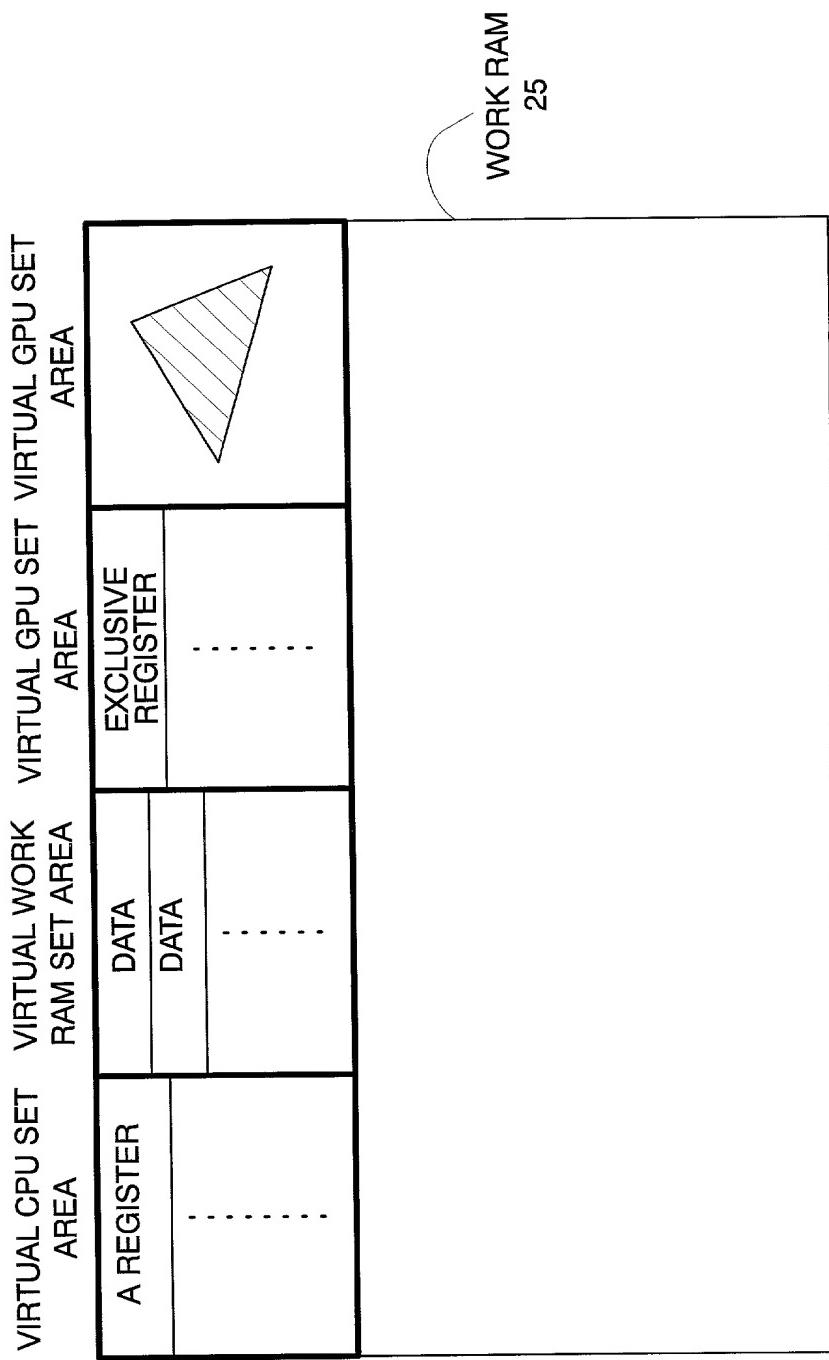
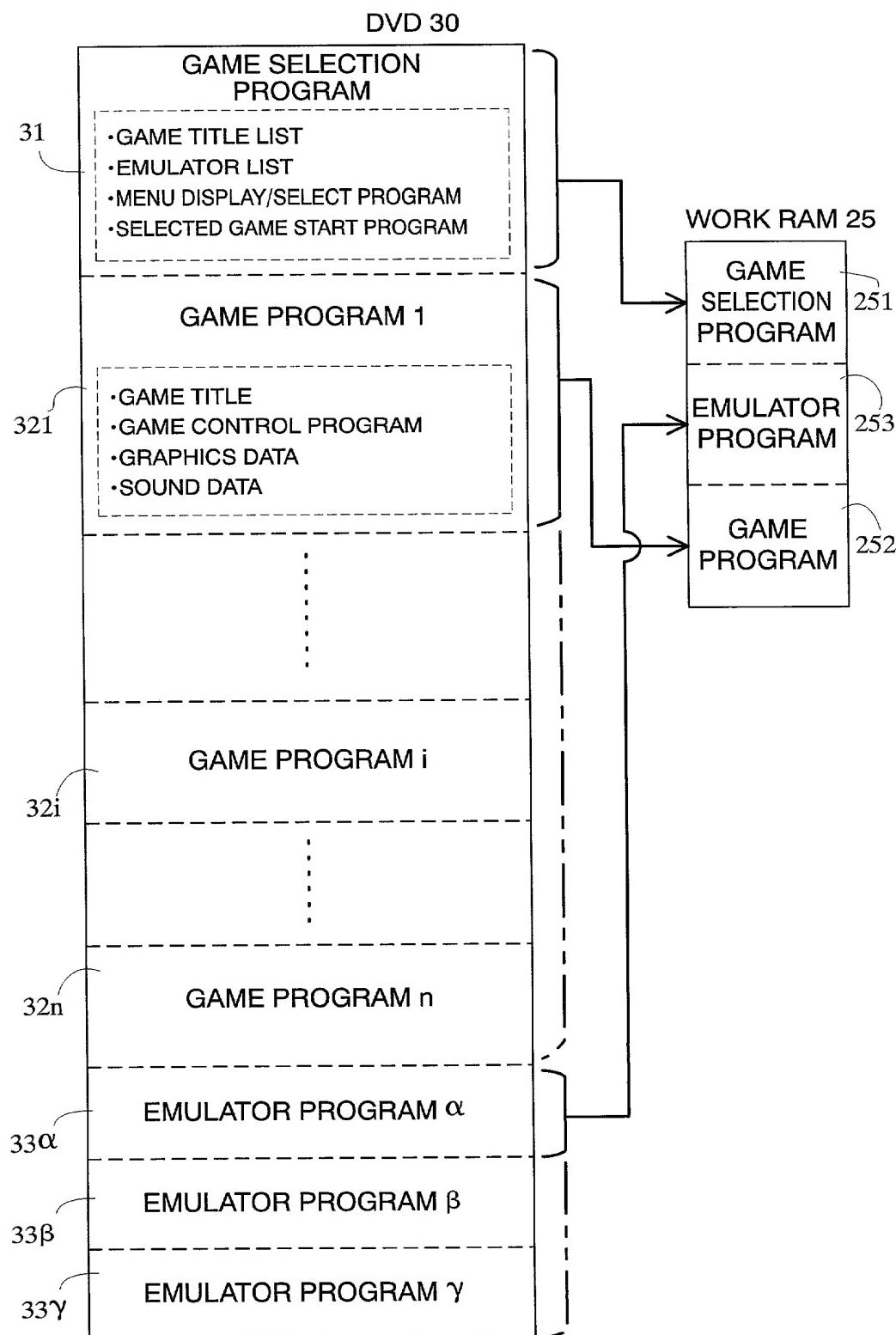


FIG.10

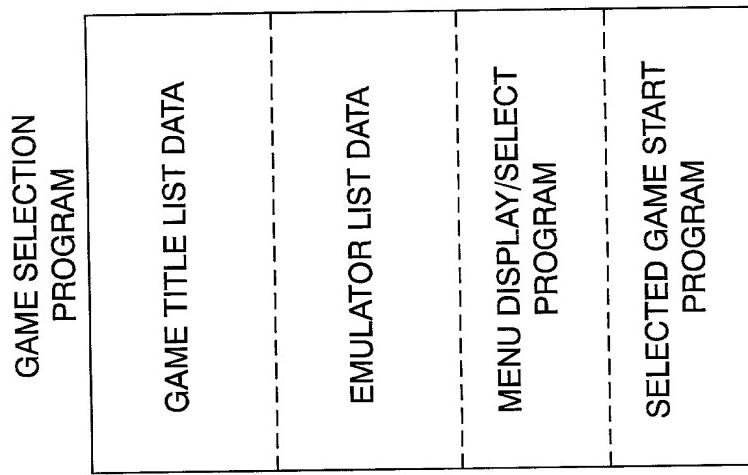


WORK RAM  
25

FIG.11



**FIG.12A**



**FIG.12B**

GAME TITLE LIST DATA	EMULATOR LIST DATA
GAME TITLE 1	EMULATOR α
⋮	⋮
GAME TITLE i	EMULATOR β
⋮	⋮
GAME TITLE n	EMULATOR γ
⋮	⋮
GAME TITLE m	⋮

FIG.13

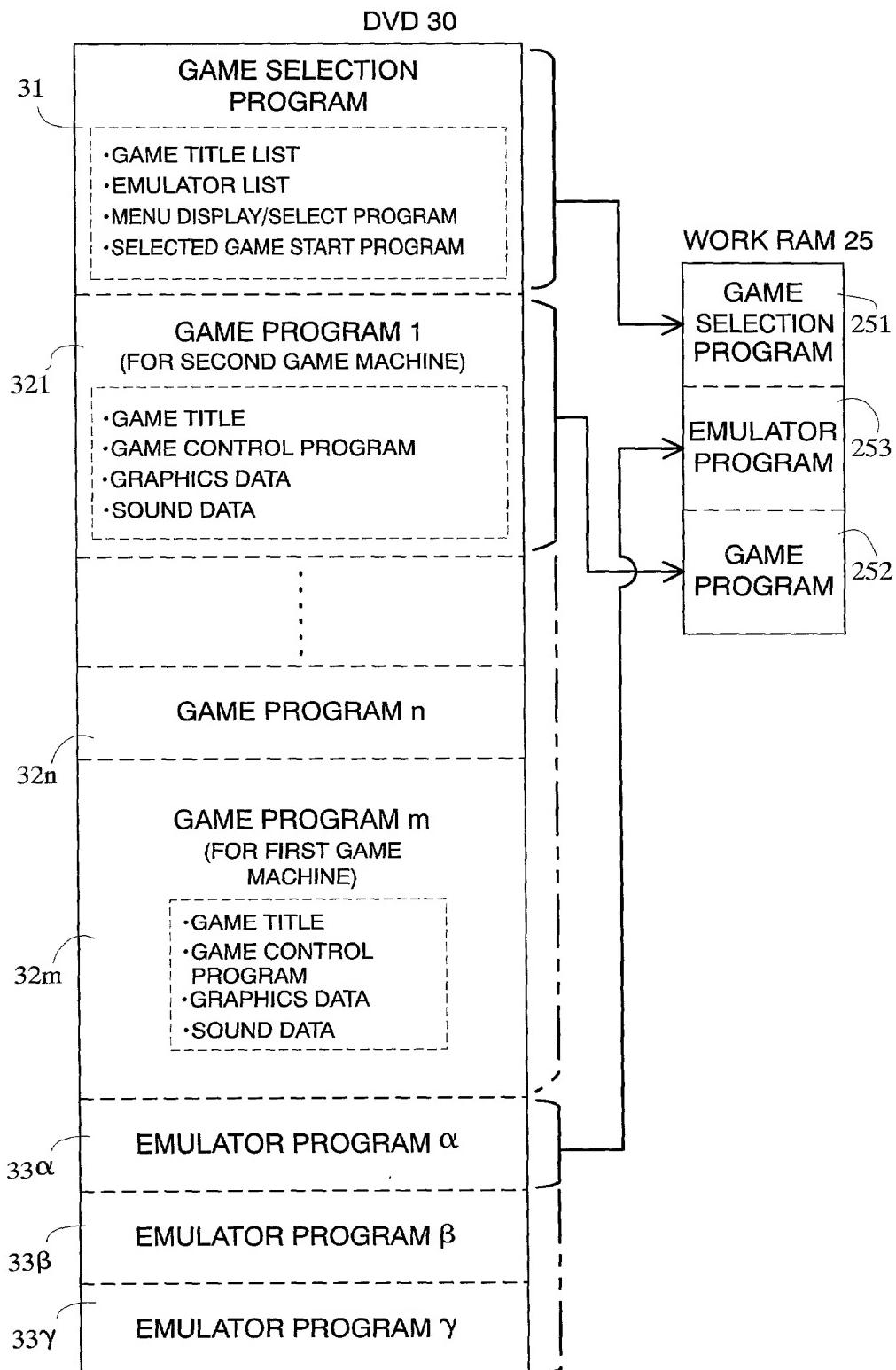
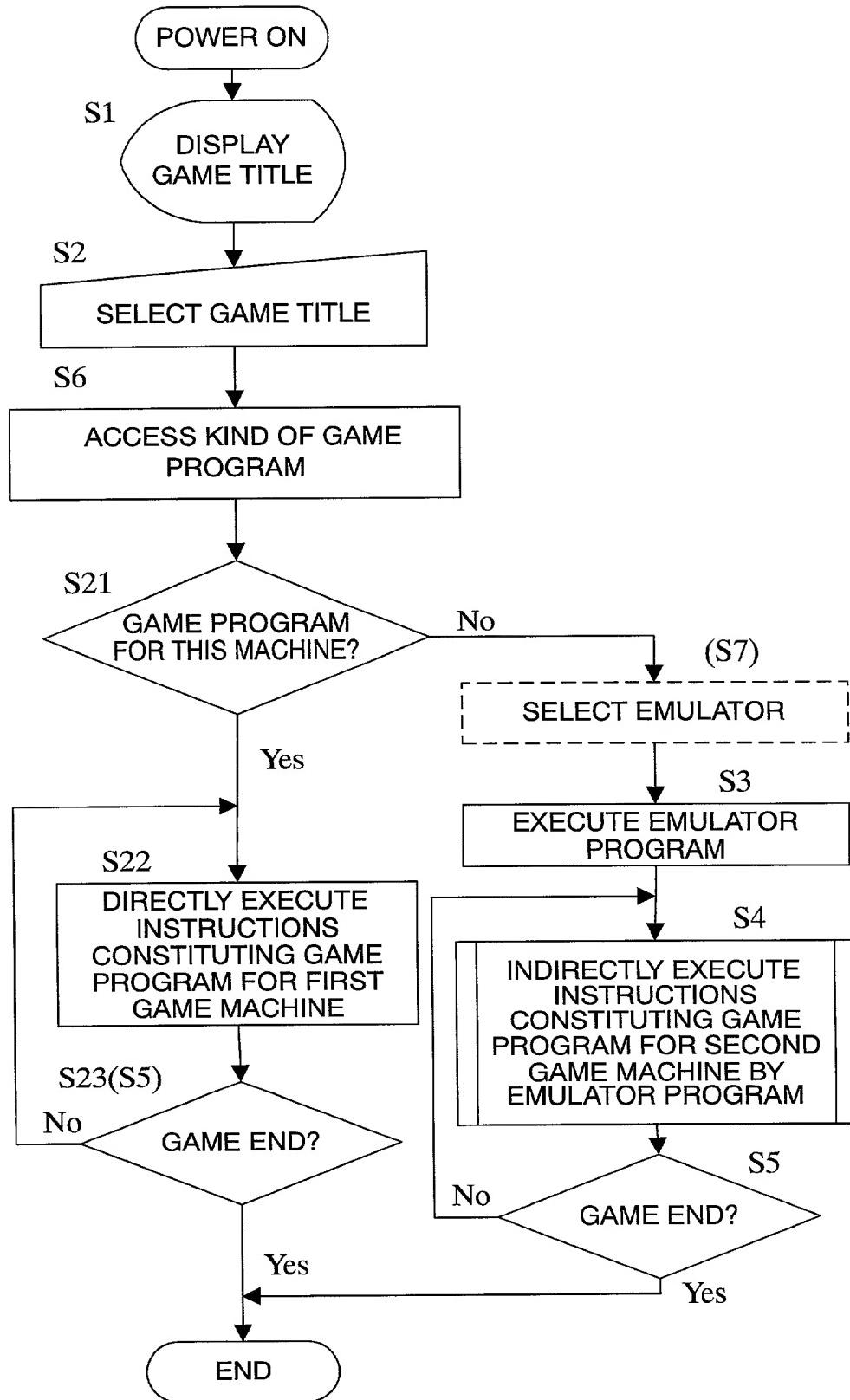
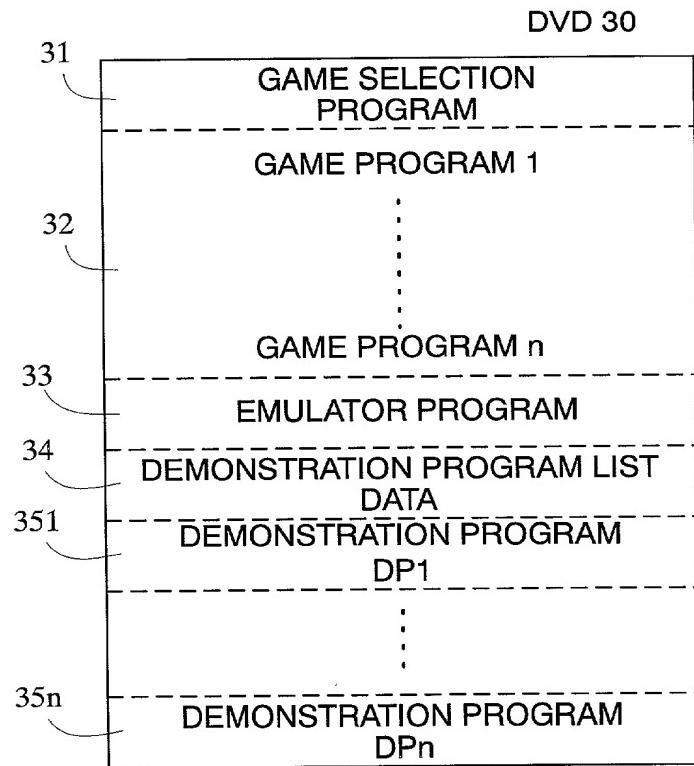


FIG.14



**FIG.15**



**FIG.16**

DEMONSTRATION PROGRAM LIST  
DATA

GAME TITLE	DEMONSTRATION PROGRAM
GAME TITLE 1	DEMONSTRATION PROGRAM DP1
⋮	⋮
GAME TITLE i	DEMONSTRATION PROGRAM DP i
⋮	⋮
GAME TITLE n	DEMONSTRATION PROGRAM DPn

FIG.17

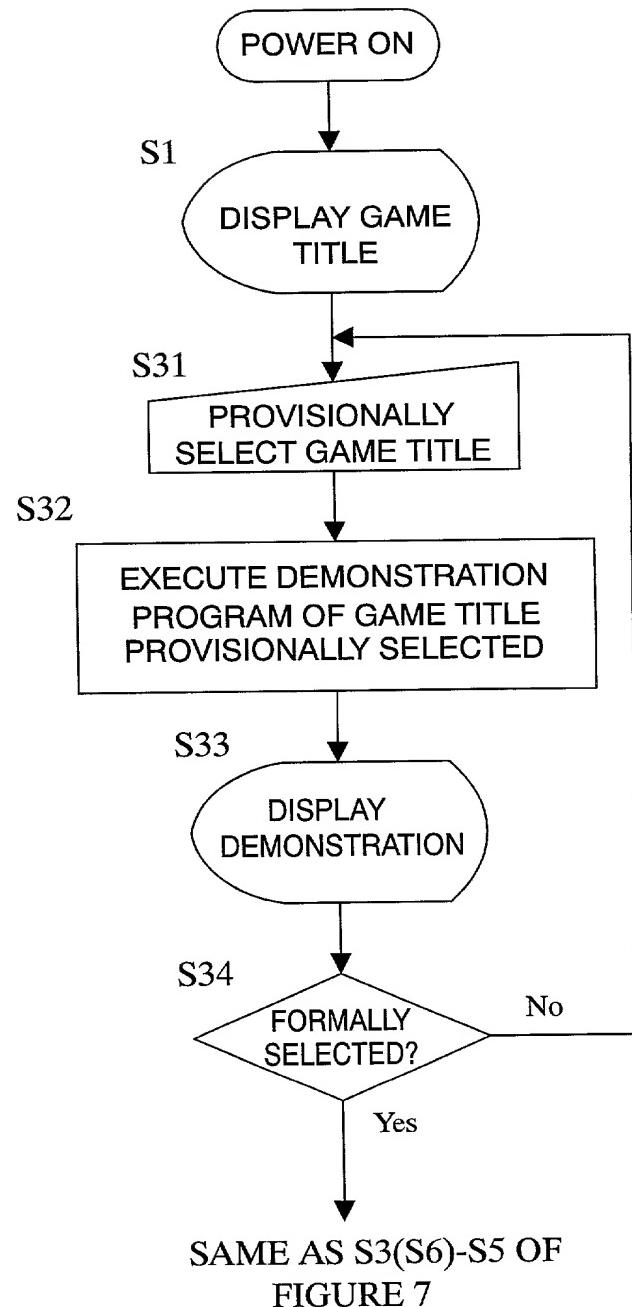


FIG.18

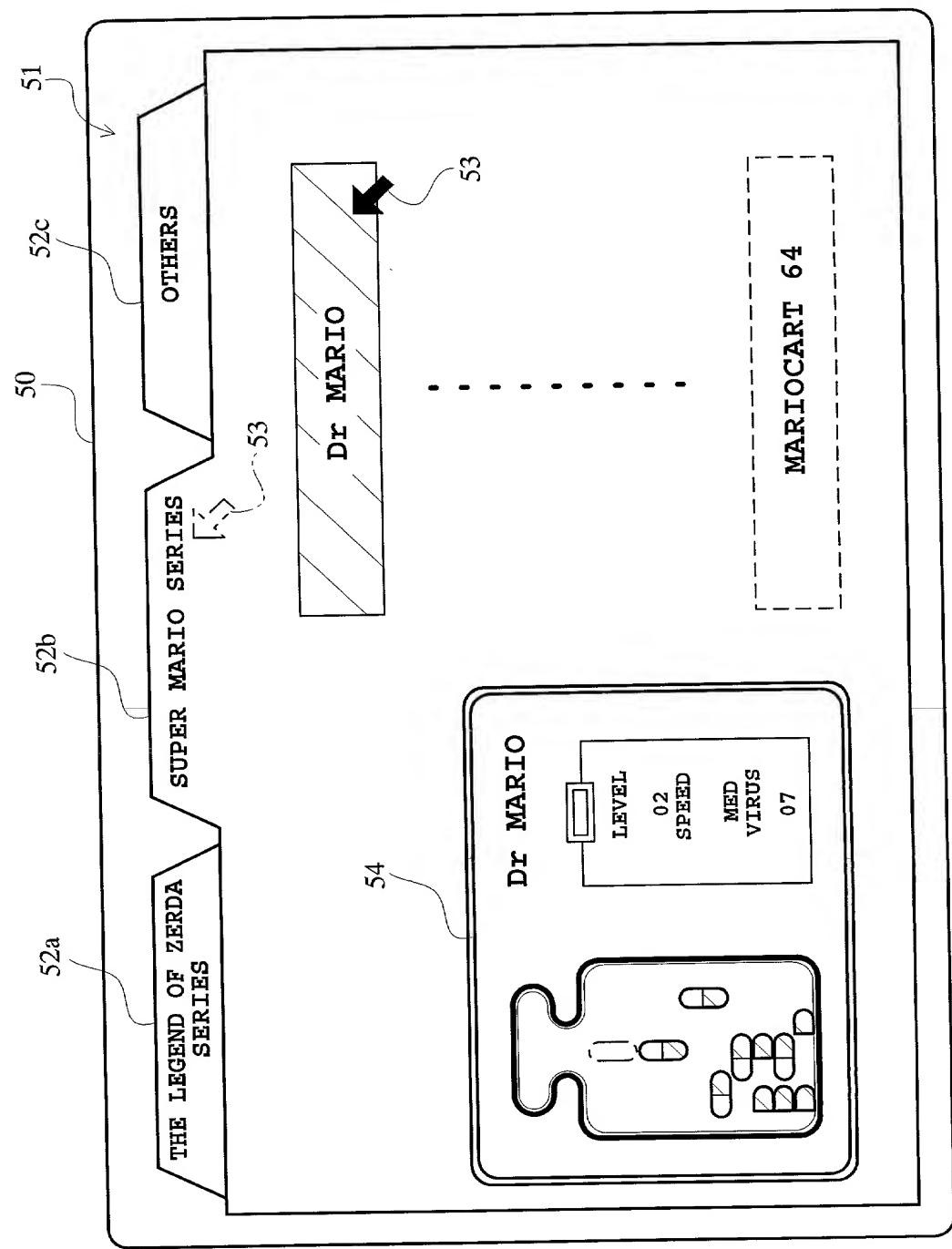


FIG.19

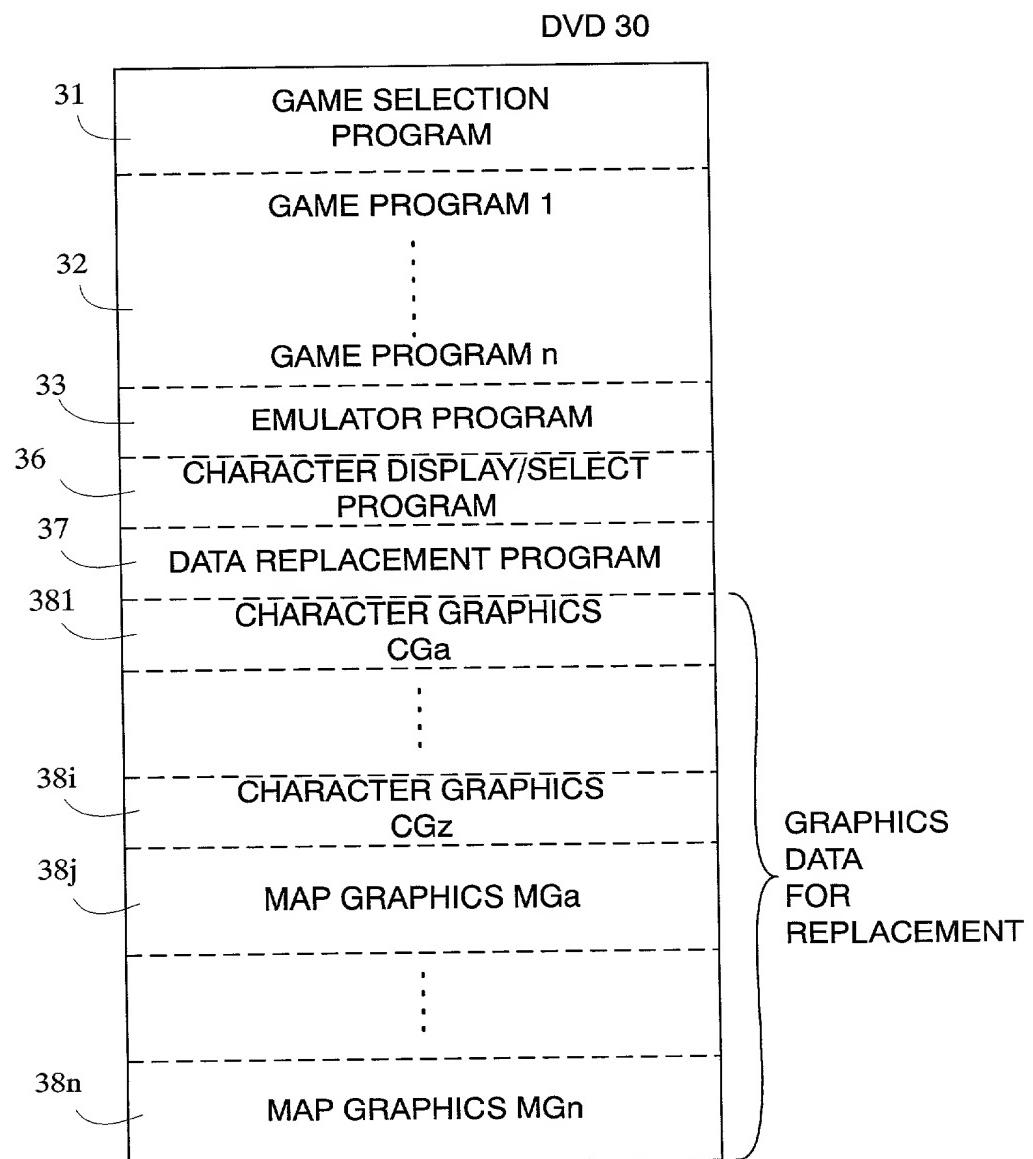


FIG.20C

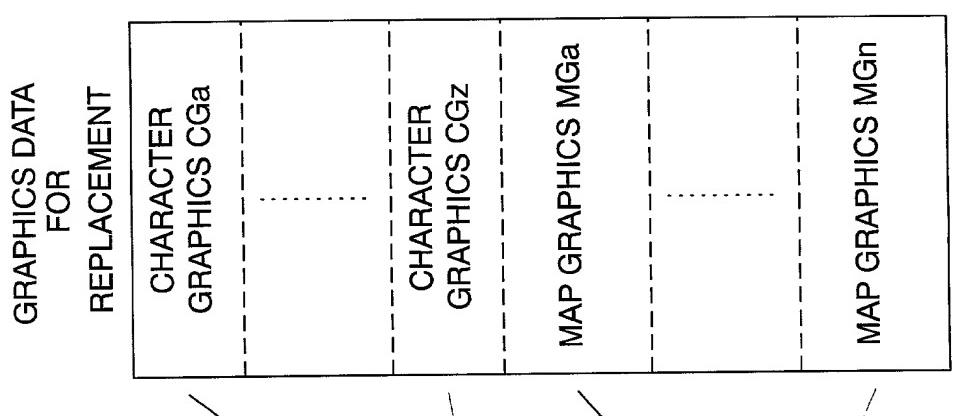


FIG.20B

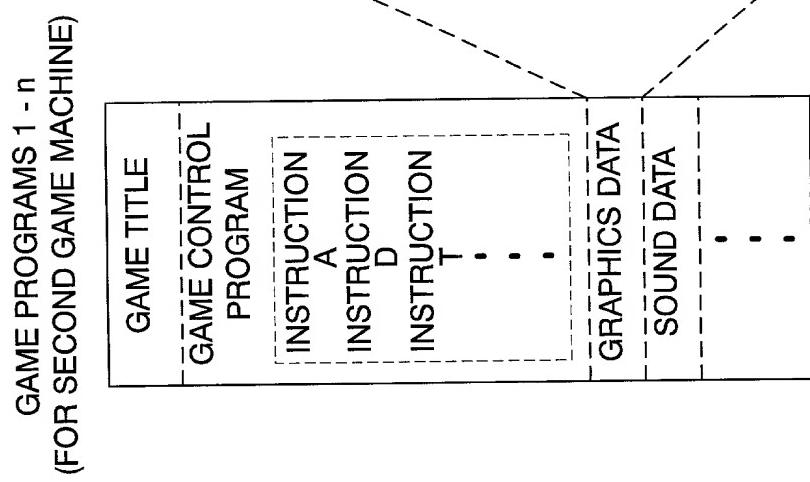


FIG.20A

FIG.21

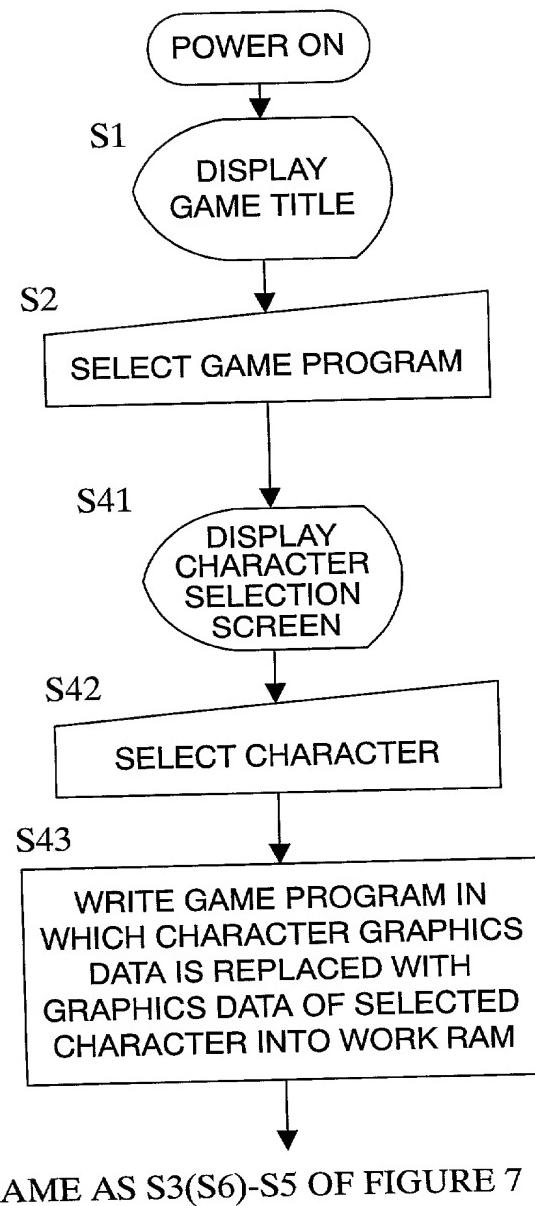


FIG.22

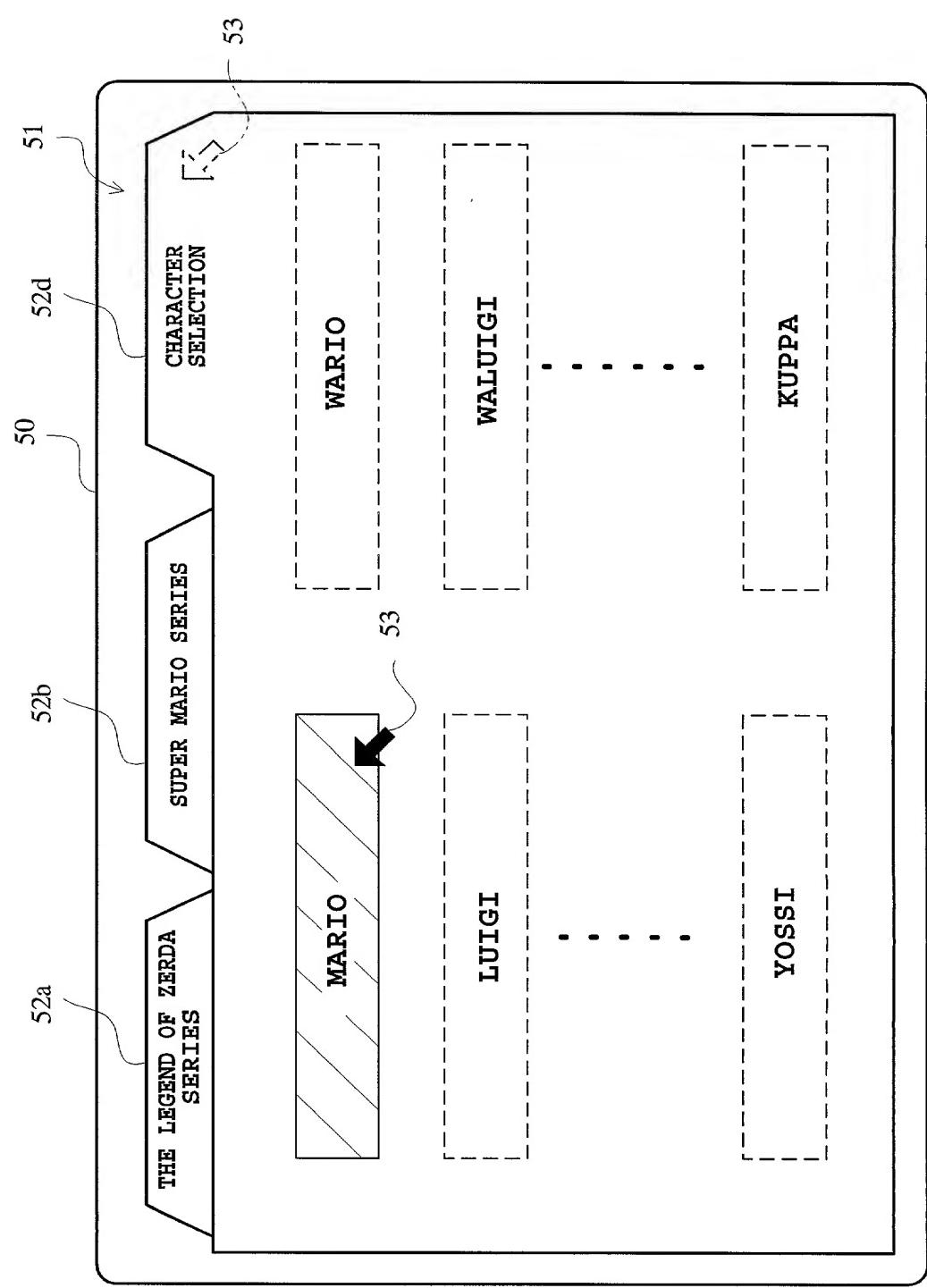


FIG.23

